*Set: All's well that ends well*

**Make sure you have typed your name and ID in the canvas of your Logisim!**

**Part 1:** *(15 minutes)*

Suppose, in the lab you are asked to construct the following circuit of figure 01. The BCD inputs are **w,x,y,z** where **w** is the MSB. The outputs are **A, B, C, D**. where,

A = w + xz + xy

B = xy’z’ +x’z +x’y

C = yz’ +yz

D = z’

Here is a twist; you found that, there is no 3 input OR gate- IC in the lab, but there is 2 input OR- gate ICs. Now redesign the circuit of Figure 01 using Logisim.

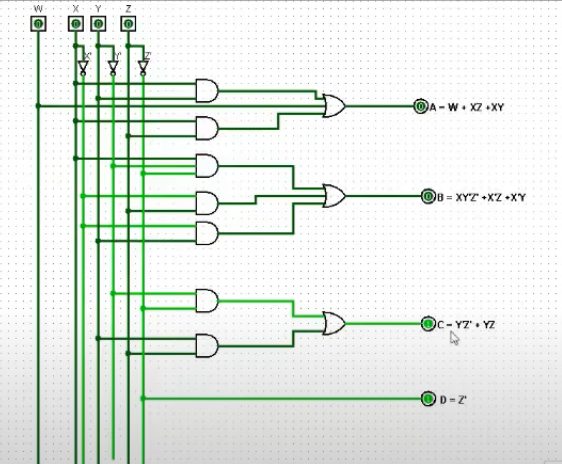


Figure-01

**Part 02:** *(5 minutes)*

Attach the screenshots of the constructed circuit at the end of this file.

Complete the **Table 01** for the given input value of w,x,y,z by observing the outputs A, B,C,D, from the simulation.

**Table 01**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Decimal Digit** | **Binary Coded**  **Decimal (BCD)** | | | | **Excess-3** | | | |
| W | X | Y | Z | A | B | C | D |
| **0** | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| **1** | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| **2** | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| **3** | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| **4** | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| **5** | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |

**Part 03:** *(5 minutes)*

Answer the following questions in your own words**.**

1. What would be the name of this design?

Ans: BCD to Excess-3

1. What would be in the question-marked boxes of the Table -01?

Ans: Binary coded decimal (BCD) , Excess-3

1. What is the name and code of this non-credit course?

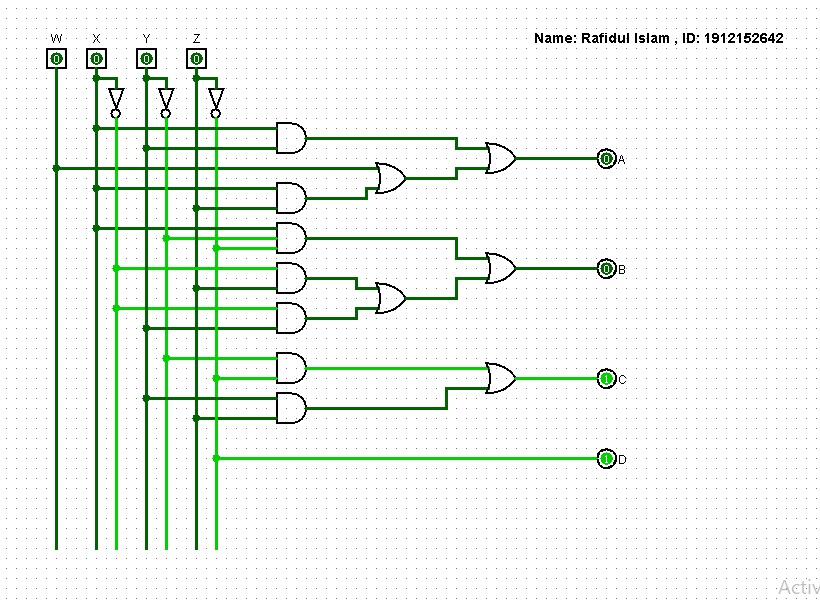
Ans: Digital Logic Design Lab, CSE231L

1. How many gates did you use?

Ans: 15

1. Is it possible to re-design the circuit using only XOR gate?

Ans: No



Part 1